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From:	Kevin J. Zilka		

Docket No.: NVIDP234_P000825 **App. No: 10/633,004**

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Practitioner's Docket No. NVIDP234/P000825 ***PATENT***

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Inderjit Singh et al.

Application No.: 10/633,004 Group No.: 2811
Filed: 07/31/2003 Examiner: Vu, H.
For: PAD OVER ACTIVE CIRUIT SYSTEM AND METHOD WITH MESHED SUPPORT STRUCTURE

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION–37 C.F.R. § 41.37)

1. Transmitted herewith, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on 6/19/06, and the Notice of Panel Decision from Pre-Appeal Brief Review mailed 08/02/06.

2. STATUS OF APPLICANT

This application is on behalf of other than a small entity.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*

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Date: 09/05/2006

Erica L. Farlow

(type or print name of person certifying)

** Only the date of filing (' 1.6) will be the date used in a patent term adjustment calculation, although the date on any certificate of mailing or transmission under ' 1.8 continues to be taken into account in determining timeliness. See ' 1.703(f). Consider "Express Mail Post Office to Addressee" (' 1.10) or facsimile transmission (' 1.6(d)) for the reply to be accorded the earliest possible filing date for patent term adjustment calculations.*

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3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is:

other than a small entity	$500.00
Appeal Brief fee due	**$500.00**

4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee	$500.00
Extension fee (if any)	$0.00
TOTAL FEE DUE	**$500.00**

6. FEE PAYMENT

Authorization is hereby made to charge the amount of $500.00 to Deposit Account No. 50-1351 (Order No. NVIDP234).

A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-1351 (Order No. NVIDP234).

Signature of Practitioner
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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	
Singh et al.	Group Art Unit: 2811
Application No. 10/633,004	Examiner: Vu, Hung K.
Filed: 07/31/2003	Date: 09/05/2006
For: PAD OVER ACTIVE CIRCUIT SYSTEM AND METHOD WITH MESHED SUPPORT STRUCTURE	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

APPEAL BRIEF (37 C.F.R. § 41.37)

This brief is in furtherance of the Notice of Appeal filed in this case on 06/19/2006, and the Notice of Panel Decision from Pre-Appeal Brief Review mailed 08/02/06.

The fees required under § 1.17, and any required petition for extension of time for filing this brief and fees therefor, are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(i)):

I REAL PARTY IN INTEREST
II RELATED APPEALS AND INTERFERENCES
III STATUS OF CLAIMS
IV STATUS OF AMENDMENTS
V SUMMARY OF CLAIMED SUBJECT MATTER
VI GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

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VII ARGUMENT

VIII CLAIMS APPENDIX

IX EVIDENCE APPENDIX

X RELATED PROCEEDING APPENDIX

The final page of this brief bears the practitioner's signature.

I REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is NVIDIA Corporation.

II RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c) (1)(ii))

With respect to other prior or pending appeals, interferences, or related judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, an appeal noted on 06/20/2006 in application serial number 10/633,021, and appeal noted on 06/19/2006 in application serial number 11/067,551 may be, but are not necessarily, related.

Since no decision(s) has been rendered in such proceeding(s), no Related Proceedings Appendix is appended hereto.

III STATUS OF CLAIMS (37 C.F.R. § 41.37(c) (1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-2, 4-18, 20-21, 27, and 29-30

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims withdrawn from consideration: None
2. Claims pending: 1-2, 4-18, 20-21, 27, and 29-30
3. Claims allowed: None
4. Claims rejected: 1-2, 4-18, 20-21, 27, and 29-30
5. Claims cancelled: 3, 19, 22-26, 28, and 31

C. CLAIMS ON APPEAL

The claims on appeal are: 1-2, 4-18, 20-21, 27, and 29-30

See additional status information in the Appendix of Claims.

IV STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

As to the status of any amendment filed subsequent to final rejection, there are no such amendments after final.

V SUMMARY OF CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

With respect to a summary of Claim 1, as shown in Figures 1-11, an integrated circuit (e.g. see item 300 of Figure 3, etc.) comprises an active circuit (e.g. see item 308 of Figure 3, etc.). See, for example, page 7, lines 4-11 et al. A metal layer is disposed, at least partially, above the active circuit, and a bond pad (e.g. see item 306 of Figure 3, etc.) is disposed, at least partially, above the metal layer. See, for example, page 7, lines 13-17; and page 8, lines 11-22 et al. Further, the metal layer (e.g. see item 412 of Figure 4, etc.) is meshed, and the metal layer is disposed, at least partially, directly above the active circuit. See, for example, page 8, line 24 – page 9, line 2 et al. In addition, the mesh (e.g. see item 604 of Figures 6A and 6B, etc.) ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process. See, for example, page 8, line 24 – page 9, line 2; and page 10, line 9 – page 11, line 8 et al. Also, the active circuit includes a plurality of transistors. See, for example, page 3, lines 10-11 et al. An entirety of at least one of the transistors is disposed directly below the bond pad. See, for example, page 8, line 24 – page 9, line 2 et al. The mesh ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process. See, for example, page 8, line 24 – page 9, line 2; and page 10, line 9 – page 11, line 8 et al.

With respect to a summary of Claim 20, as shown in Figures 1-11, an integrated circuit (e.g. see item 300 of Figure 3, etc.) comprises an active circuit means (e.g. see item 308 of Figure 3, etc.) for processing electrical signals. See, for example, page 7, lines 4-11 et al. A metal layer is disposed, at least partially, above the active circuit means (e.g. see item 308 of Figure 3, etc.) and includes a mesh means (e.g. see item 604 of Figures 6A and 6B, etc.) for preventing damage incurred during a bonding process. See, for example, page 8, line 24 – page 9, line 2 et al. A bond pad (e.g. see item 306 of Figure 3, etc.) is disposed, at least partially, above the metal layer. See, for example, page 7, lines 13-17; and page 8, lines 11-22 et al. Further, the metal layer is disposed, at least partially, directly above the active circuit means (e.g. see item 308 of Figure 3, etc.). See, for example, page 8, line 24 – page 9, line 2 et al. In addition, the mesh means (e.g. see item 604 of Figures 6A and 6B, etc.) ensures that bonds are capable of being placed over the active circuit means (e.g. see item 308 of Figure 3, etc.) without damage thereto during a

bonding process. See, for example, page 8, line 24 – page 9, line 2; and page 10, line 9 – page 11, line 8 et al. Also, the active circuit means (e.g. see item 308 of Figure 3, etc.) includes a plurality of transistors. See, for example, page 3, lines 10-11 et al. An entirety of at least one of the transistors is disposed directly below the bond pad (e.g. see item 306 of Figure 3, etc.). See, for example, page 8, line 24 – page 9, line 2 et al. The mesh means (e.g. see item 604 of Figures 6A and 6B, etc.) ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process. See, for example, page 8, line 24 – page 9, line 2; and page 10, line 9 – page 11, line 8 et al.

With respect to a summary of Claim 21, as shown in Figures 1-11, an integrated circuit (e.g. see item 300 of Figure 3, etc.) comprises a semiconductor structure including an active circuit (e.g. see item 308 of Figure 3, etc.) including an input/output (I/O) bus (e.g. see item 304 of Figure 3, etc.) and a plurality of transistors forming a core of circuits (e.g. see item 302 of Figure 3, etc.). See, for example, page 3, lines 10-11; and page 7, lines 4-11 et al. Further, a plurality of vertically spaced underlying metal layers (e.g. see item 406 of Figure 4, etc.) are disposed, at least partially, under the active circuit (e.g. see item 308 of Figure 3, etc.) and around a periphery thereof. Each of the underlying metal layers are in electrical communication by way of a plurality of underlying vias (e.g. see item 408 of Figure 4, etc.) with the active circuit and other underlying metal layers (e.g. see item 406 of Figure 4, etc.). See, for example, page 8, lines 1-9 et al. In addition, a meshed interconnect metal layer (e.g. see item 412 of Figure 4, etc.) is disposed, at least partially, above the I/O bus of the active circuit and around a periphery thereof (e.g. see Figure 4, etc.). See, for example, page 8, lines 11-18 et al. The interconnect metal layer is in electrical communication with the underlying metal layers (e.g. see item 406 of Figure 4, etc.) by way of a plurality of additional vias (e.g. see item 414 of Figure 4, etc.). See, for example, page 8, lines 11-18 et al. Additionally, an inter-metal dielectric layer (e.g. see item 416 of Figure 4, etc.) is disposed, at least partially, above the interconnect metal layer. The inter-metal dielectric layer (e.g. see item 416 of Figure 4, etc.) is constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material. See, for example, page 8, lines 11-18 et al. Also, a top metal layer is disposed, at least partially, above the inter-metal dielectric layer (e.g. see item 416 of Figure 4, etc.). The top metal layer for serves as a bond pad (e.g. see item 306 of Figure 3, etc.), where the top metal layer is in electrical communication with the interconnect metal layer by way of a plurality of

interconnect vias (e.g. see item 420 of Figure 4, etc.). See, for example, page 8, lines 20-22 et al. Further, a passivation layer is disposed (e.g. see item 510 of Figure 5, etc.), at least partially, above the top metal layer. See, for example, page 9, lines 19-21 et al. The interconnect metal layer is meshed for preventing damage incurred during a bonding process. See, for example, page 8, line 24 – page 9, line 2 et al. In addition, the metal layer is disposed, at least partially, directly above the active circuit. See, for example, page 8, lines 11-18 et al. The mesh ensures that bonds are capable of being placed over the active circuit without damage thereto during the bonding process. See, for example, page 8, line 24 – page 9, line 2 et al. Also, an entirety of at least one of the transistors is disposed directly below the bond pad (e.g. see item 306 of Figure 3, etc.). See, for example, page 8, line 6 – page 9, line 2 et al. The mesh ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process. See, for example, page 8, line 24 – page 9, line 2 et al.

VI GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Following, under each issue listed, is a concise statement setting forth the corresponding ground of rejection.

Issue # 1: The Examiner has rejected Claims 1-2, 4-18, 20-21, 27, and 29-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Issue # 2: The Examiner has rejected Claims 1, 4-18, 20, 27, and 29-30 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589).

Issue # 3: The Examiner has rejected Claims 2, and 21 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589), and in further view of Applicant's Admitted Prior Art of Figures 1 and 2.

VII ARGUMENT (37 C.F.R. § 41.37(c)(1)(vii))

The claims of the groups noted below do not stand or fall together. In the present section, appellant explains why the claims of each group are believed to be separately patentable.

Issue # 1:

The Examiner has rejected Claims l-2, 4-18, 20-21, 27, and 29-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Specifically, the Examiner argues that the specification does not disclose an entirety of at least one of the transistors being disposed directly below the bond pad, as recited in Claim 1, 20 and 21. On page 3, lines 10-11 of the originally filed application, it is disclosed that "the active circuit may include a plurality of transistors." Further, Claim 21 of the originally filed application discloses "a plurality of transistors forming a core of circuits." Still yet, on page of 7, lines 16-17 of the originally filed application, it is disclosed that "the bond pads **306** may be disposed above the core **302**, and/or any other part of the active circuit **308**." By virtue of this and other disclosure, appellant's claims clearly meet the written description requirement.

Issue # 2:

The Examiner has rejected Claims 1, 4-18, 20, 27, and 29-30 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589).

Group #1 - Claims 1, 4-16, 20, 27, and 29-30

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The

teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on appellant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

With respect to the first element of the *prima facie* case of obviousness, the Examiner states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the integrated circuit of Suzuki et al. having the metal layer defined a mesh, such as taught by Tanaka in order to further improve the mechanical strength and to further enhance the effects for suppressing crack formation in the insulation interlayer so that it inherently prevents the damage to the active circuit and/or the at least one transistor during the bonding process. Appellant respectfully disagrees with this proposition, especially in view of the vast evidence to the contrary.

Specifically, it is noted that Tanaka merely addresses the problem of arranging bonding pads with high density, since a first electrode layer must have a large area in order to secure the bonding area, due to disconnection from bumps of aluminum wiring, etc. Note col. 1, lines 15-45 from Tanaka. Therefore, it is clear that Tanaka simply does not address the problem of bonding-related damage to the active circuit.

Still yet, it is noted that Suzuki does not even mention bonding, let alone the problem of bonding-related damage to the active circuit. Specifically, Suzuki merely teaches a technique for dealing with an increase of stress associated with increasing a height of a multilevel wiring layer structure. For example, Suzuki discloses that "if an interlayer insulating layer of SiOC is disposed between an organic insulating layer and a silicon oxide layer, the generation of stress and the like to be caused by a difference of a physical constant between the upper and lower level layers can be suppressed" (col. 6. lines 11-15). Thus, Suzuki simply does not even address the problem of bonding-related damage to the active circuit.

To this end, neither prior art references even teaches the problem solved by appellant. See *Eibel Process Co. v Minnesota & Ontario Paper Co.*, 261 US 45 (1923). Therefore, for at least the reasons set forth hereinabove, the first element of the *prima facie* case of obviousness has simply not been met.

More importantly, with respect to the third element of the *prima facie* case of obviousness, the Examiner relies on Figure 1 from Suzuki to make a prior art showing of appellant's claimed structure "wherein the [metal layer]... ensures that bonds are capable of being placed over the active circuit" (see this or similar, but not necessarily identical language in each of the independent claims).

Appellant respectfully disagrees with this assertion. First, as mentioned above, Suzuki does not even mention bonding, let alone the problem of bonding-related damage to the active circuit. Specifically, it is noted that Suzuki merely teaches a technique for dealing with an increase of stress associated with increasing a height of a multilevel wiring layer structure. For example, Suzuki discloses that "if an interlayer insulating layer of SiOC is disposed between an organic insulating layer and a silicon oxide layer, the generation of stress and the like to be caused by a difference of a physical constant between the upper and lower level layers can be suppressed" (col. 6. lines 11-15).

Such disclosure simply does not "ensure that bonds are capable of being placed over the active circuit," let alone "without damage thereto during a bonding process" (emphasis added), as claimed. It appears that the Examiner has admitted to not identifying the above emphasized claim language in the prior art. It also noted that the Examiner appears to rely on an inherency argument by arguing that the resultant combination *inherently* prevents the damage to the active circuit and/or the at least one transistor during the bonding process.

In response, appellant asserts that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981). "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999)

Appellant respectfully asserts that the claimed "mesh [which] ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process" would be *unobvious* in view of the proposed prior art combination since only appellant teaches and claims the novel use of such meshed metal layer structure for the specific purpose of ensuring that bonds are capable of being placed over the active circuit without damage thereto during a bonding process, as claimed.

In summary, none of the references relied upon by the Examiner even suggest a mesh, as claimed by appellant, to ensure that bonds are capable of being placed over the active circuit without damage thereto during a bonding process. For these reasons, appellant respectfully asserts that the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above.

A notice of allowance or a specific prior art showing of all of appellant's claim limitations, in combination with the remaining claim elements, is respectfully requested.

Group #2 – Claim 17

With respect to such claim, it is noted that the Examiner's rejection is still deficient. Specifically, the Examiner relies on Figures 7A and those shown below from Tanaka to meet appellant's claimed "wherein the interconnect vias include at least two spaced rows for each of the first portions."

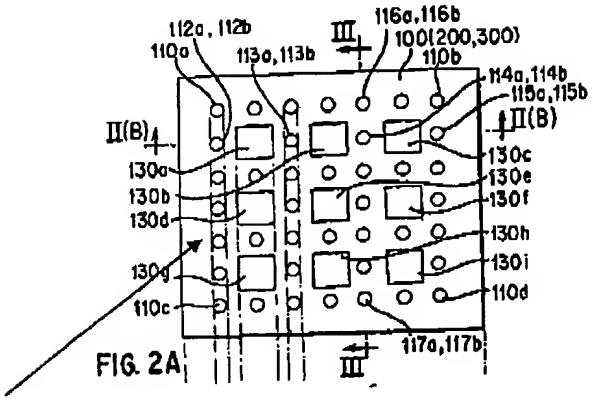

FIG. 2A

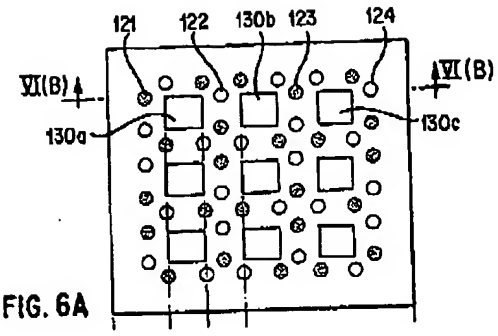

FIG. 6A

Specifically, the Examiner argues that "interconnect vias (110a-c and 120a-c) include at least two spaced rows for each of the first portions." Appellant respectfully disagrees, as it appears that the Examiner has simply not taken into consideration the full weight of appellant's claim language. For example, appellant's claimed "first portions" are clearly defined as a plurality of substantially linear first portions which intersect a plurality of substantially linear second portions to define a matrix of openings (note intervening Claims 12-13). Thus, it is clear that appellant's claimed "first portions" each correlate with one of the rows annotated above by the arrow.

To this end, in no row of Tanaka is there any "at least two spaced rows" of "interconnect vias," as claimed. In fact, as noted in Figure 6A from Tanaka above, the rows thereof are not spaced (note the crowding and the interconnects positioned in the "second portions," which intersect the first portions, etc.). Appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above.

Group #3 – Claim 18

With respect to such claim, it is noted that the Examiner's rejection is still deficient. Specifically, the Examiner relies on Figures 7A and those shown below from Tanaka to meet appellant's claimed technique "wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions."

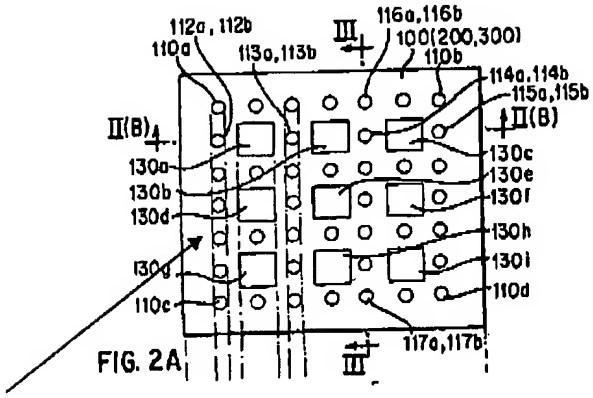

FIG. 2A

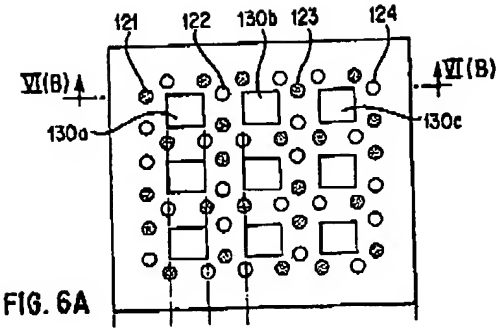

FIG. 6A

Specifically, the Examiner argues that "interconnect vias (110a-c and 120a-c) include at least two spaced rows for each of the first portions." Appellant respectfully disagrees, as it appears that the Examiner has simply not taken into consideration the full weight of appellant's claim language. For example, appellant's claimed "first portions" are clearly defined as a plurality of substantially linear first portions which intersect a plurality of substantially linear second portions to define a matrix of openings (note intervening Claims 12-13). Thus, it is clear that appellant's claimed "first portions" each correlate with one of the rows annotated above by the arrow.

To this end, in no row of Tanaka is there any "at least two spaced rows" of "interconnect vias" formed thereon and "wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions," as claimed. In fact, as noted in Figure 6A from Tanaka above, the rows thereof are not enlarged to accommodate any two spaced rows (note the crowding and the interconnects positioned in the "second portions," which intersect the first portions, etc.).

Again, only appellant teaches and claims mesh first portions that have enlarged widths so that two spaced rows of vias are better accommodated. Again, appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above.

Issue # 3:

The Examiner has rejected Claims 2, and 21 under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (US Patent Number: 6,707,156) in view of Tanaka (US Patent Number: 6,100,589), and in further view of Applicant's Admitted Prior Art of Figures 1 and 2.

Group #1 – Claim 2

Appellant respectfully asserts that such claims are not met by the prior art for the reasons argued with respect to Issue #2, Group #1.

Again, appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above.

Group #2 – Claim 21

The Examiner argues that "Applicant's Admitted Prior Art of Figures 1-2 disclose ... a plurality of ... metal layers (M1-M4), at least partially, under the active circuit." Whether this is true or not, the Examiner has still not considered the full weight of appellant's claims. Note Figure 2 below.

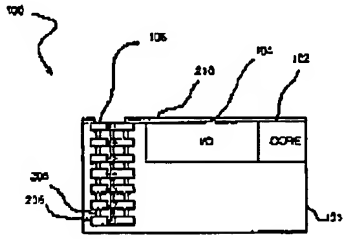

FIG. 2
(Prior Art)

The Examiner argues that the foregoing figure discloses an active circuit including an input/output bus and metal layers, at least partially, under the active circuit.

However, the Examiner's art and arguments simply do not address applicant's claimed "meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit," as claimed. Again, appellant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, when combined, fail to teach or suggest all of the claim limitations, as noted above.

VIII CLAIMS APPENDIX (37 C.F.R. § 41.37(c)(1)(viii))

The text of the claims involved in the appeal (along with associated status information) is set forth below:

1. (Previously Presented) An integrated circuit, comprising:

an active circuit;

a metal layer disposed, at least partially, above the active circuit; and

a bond pad disposed, at least partially, above the metal layer;

wherein the metal layer is meshed;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the mesh ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process;

wherein the active circuit includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the mesh ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

2. (Original) The integrated circuit as recited in claim 1, wherein the active circuit includes an input/output (I/O) bus.

3. (Cancelled)

4. (Original) The integrated circuit as recited in claim 1, wherein the metal layer includes an interconnect metal layer.

5. (Original) The integrated circuit as recited in claim 4, wherein the interconnect metal layer interconnects the bond pad with a plurality of underlying metal layers.

6. (Previously Presented) The integrated circuit as recited in claim 5, wherein each of the underlying metal layers is in electrical communication by way of a plurality of vias.

7. (Original) The integrated circuit as recited in claim 1, wherein the metal layer includes a plurality of openings.

8. (Original) The integrated circuit as recited in claim 7, wherein the openings are adapted for facilitating an interlock between the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

9. (Original) The integrated circuit as recited in claim 8, wherein the inter-metal dielectric layer is constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material.

10. (Original) The integrated circuit as recited in claim 7, wherein the openings are completely enclosed around a periphery thereof.

11. (Original) The integrated circuit as recited in claim 7, wherein the openings have a substantially square configuration.

12. (Original) The integrated circuit as recited in claim 7, wherein the openings define a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect.

13. (Original) The integrated circuit as recited in claim 12, wherein the openings define a matrix of openings.

14. (Original) The integrated circuit as recited in claim 13, wherein a plurality of interconnect vias are formed in rows along the first portions.

15. (Original) The integrated circuit as recited in claim 14, wherein the interconnect vias are spaced along a length of the first portions.

16. (Original) The integrated circuit as recited in claim 15, wherein the interconnect vias include one single row for each of the first portions.

17. (Original) The integrated circuit as recited in claim 15, wherein the interconnect vias include at least two spaced rows for each of the first portions.

18. (Original) The integrated circuit as recited in claim 17, wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions.

19. (Cancelled)

20. (Previously Presented) An integrated circuit, comprising:

an active circuit means for processing electrical signals;

a metal layer disposed, at least partially, above the active circuit means and including a mesh means for preventing damage incurred during a bonding process; and

a bond pad disposed, at least partially, above the metal layer;

wherein the metal layer is disposed, at least partially, directly above the active circuit means;

wherein the mesh means ensures that bonds are capable of being placed over the active circuit means without damage thereto during a bonding process;

wherein the active circuit means includes a plurality of transistors, and an entirety of at least one of the transistors is disposed directly below the bond pad, and the mesh means ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

21. (Previously Presented) An integrated circuit, comprising:

a semiconductor structure including an active circuit including an input/output (I/O) bus and a plurality of transistors forming a core of circuits;

a plurality of vertically spaced underlying metal layers disposed, at least partially, under the active circuit and around a periphery thereof, wherein each of the underlying metal layers are in electrical communication by way of a plurality of underlying vias with the active circuit and other underlying metal layers;

a meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit and around a periphery thereof, the interconnect metal layer being in electrical communication with the underlying metal layers by way of a plurality of additional vias;

an inter-metal dielectric layer disposed, at least partially, above the interconnect metal layer, the inter-metal dielectric layer constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material;

a top metal layer disposed, at least partially, above the inter-metal dielectric layer, the top metal layer for serving as a bond pad, the top metal layer being in electrical communication with the interconnect metal layer by way of a plurality of interconnect vias; and

a passivation layer disposed, at least partially, above the top metal layer.

wherein the interconnect metal layer is meshed for preventing damage incurred during a bonding process;

wherein the metal layer is disposed, at least partially, directly above the active circuit;

wherein the mesh ensures that bonds are capable of being placed over the active circuit without damage thereto during the bonding process;

wherein an entirety of at least one of the transistors is disposed directly below the bond pad, and the mesh ensures that at least one of the bonds is capable of being placed over the at least one transistor without damage thereto during the bonding process.

22. - 26. (Cancelled)

27. (Previously Presented) The integrated circuit as recited in claim 1, wherein the metal layer is disposed, at least partially, above the active circuit along a vertical axis.

28. (Cancelled)

29. (Previously Presented) The integrated circuit as recited in claim 8, wherein the inter-metal dielectric layer is constructed from a low-K dielectric material.

30. (Previously Presented) The integrated circuit as recited in claim 8, wherein the inter-metal dielectric layer is constructed from a fluorinated silica glass (FSG) material.

31. (Cancelled)

IX EVIDENCE APPENDIX (37 C.F.R. § 41.37(c)(1)(ix))

There is no such evidence.

X RELATED PROCEEDING APPENDIX (37 C.F.R. § 41.37(c)(1)(x))

Since no decision(s) has been rendered in such proceeding(s), no material is included in this Related Proceedings Appendix.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 971-2573. For payment of any additional fees due in connection with the filing of this paper, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1351 (Order No. NVIDP234/P000825).

Respectfully submitted,

By: _____ Date: 9/5/06

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